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(54) Title: INSULATED BOND WIRE ASSEMBLY PROCESS TECHNOLOGY FOR INTEGRATED CIRCUITS

(57) Abstract: An insulated bond wire to connect integrated circuits to each other or to substrates. Insulated bond wires may allow bond wires connecting integrated circuits and substrates to cross without shorting. Because bond wires may be crossed, integrated circuit assemblies with crossing bond wires may not need to be redesigned to avoid the wire crossings. In addition, insulated bond wires may also allow for closer spacing between bond wires due to reduced electronic interference between the wires. Closer spacing may allow for more input and output ports on an integrated circuit and thus increase its functionality.

**INSULATED BOND WIRE ASSEMBLY PROCESS TECHNOLOGY FOR
INTEGRATED CIRCUITS**

FIELD OF THE INVENTION

- 5 [0001] The present invention relates to integrated circuits and in particular, insulated bond wires.

BACKGROUND OF THE RELATED ART

- [0002] Integrated circuit assemblies may use bare bond wires to connect to each other and to underlying substrates. The bare bond wires may connect circuits on integrated 10 circuits to circuits on substrates or other integrated circuits through types of bond pads, such as metal pads and lead frame posts. The bare bond wires may be made of gold, silver, aluminum, or copper.

- [0003] To install the bare bond wires, a cutting machine may cut ultra thin bare bond wire into predetermined lengths. A bonding machine may then ultrasonically bond each 15 end of the bare bond wire to the bond pad or lead frame post on either an integrated circuit or a substrate. The bond pads may be 100 microns by 100 microns square. The minimum distance the bonding machine can move between the bond pads usually restricts a minimum spacing between the bare bond wires. After making the needed connections with the bare bond wires, hot plastic may be molded over the integrated circuit assembly 20 and cooled.

- [0004] Using bare bond wires on integrated circuits and substrates has many disadvantages. Because the bare bond wires may short if they come in contact with each 25 other, the integrated circuits are typically designed such that the bare bond wires connecting one integrated circuit to another do not cross each other. A change in design of one integrated circuit or substrate may mean that the other integrated circuits or substrates in the integrated circuit assembly have to be redesigned to keep the bare bond wires from crossing. The redesign of the integrated circuits and substrates may be especially tedious if different vendors manufacture their components.

- [0005] The bare bond wires that sag may pose additional problems. If the bare bond 30 wires sag into other bare bond wires, the touching bare bond wires may short. In addition, if the bare bond wires sag into an edge of the integrated circuit, the bare bond wires may short as well. The problems with the bare bond wires sagging may become worse if hot plastic is molded over the integrated circuit assembly that uses the bare bond wires. If the

hot plastic is molded over the integrated circuit assembly, the hot plastic may push the bare bond wires together, potentially causing them to short. Also, the hot plastic may push the bare bond wires into the edge of the integrated circuit causing the bare bond wires to short.

- 5 [0006] Another potential problem encountered by the bare bond wires is electronic interference. Current in the bare bond wires may cause electronic interference with the current in neighboring bare bond wires. Accordingly, the bare bond wires may need to be spaced far enough apart to minimize the effects of electronic interference from neighboring bare bond wires.

10 **BRIEF DESCRIPTION OF THE DRAWINGS**

[0007] Fig. 1 shows an embodiment of the invention having an integrated circuit connected to a substrate through an insulated bond wire.

[0008] Fig. 2 is a flowchart showing an embodiment of the invention in the form of a method for connecting insulating material to bare bond wire.

15 [0009] Fig. 3 shows an embodiment of the invention having two integrated circuits connected to each other and to an underlying substrate through multiple insulated bond wires.

[0010] Fig. 4 shows a close-up of a ball bond between an insulated bond wire and a lead frame post.

20 [0011] Fig. 5 shows an embodiment of the invention with two integrated circuits connected to each other and an underlying substrate through multiple insulated bond wires placed very close together.

DETAILED DESCRIPTION OF THE INVENTION

[0012] The following description makes reference to numerous specific details in order 25 to provide a thorough understanding of the present invention. However, it is to be noted that not every specific detail need be employed to practice the present invention.

Additionally, well-known details, such as particular materials or methods, have not been described in order to avoid obscuring the present invention.

[0013] Referring to Fig. 1, an embodiment of the invention using insulated bond wires 30 to connect an integrated circuit to an underlying substrate is shown. Bare bond wire materials may be gold, silver, aluminum, or copper. Insulated bond wire 5, having bare bond wire 7 coated in insulating material 6, such as a polymer, may be used to connect the integrated circuit 3 to the underlying substrate 2. Possible insulating materials 6 include,

but are not limited to, polyvinyl, polytetrafluoroethylene, fluorinated ethylene propylene, and polyimide. The underlying substrate 2 may also be a second integrated circuit. Examples of the underlying substrates 2 that may be connected to the integrated circuit 3 include, but are not limited to, printable circuit boards, aluminum lead frames, and fine pitch ball grid arrays. To connect the integrated circuit 3 to the underlying substrate 2, a first end of the insulated bond wire 5 may be connected to a lead frame post 9 (a type of bond pad) on the underlying substrate 2, and an end of the insulated bond wire 5 may be connected to the bond pad 10 on the integrated circuit 3. The bond pads 10 on the integrated circuit 3 may be a type of address pin, such as, but not limited to power supply pins, input pins, output pins, input/output pins, control pins, or clock pins. The bond pad 10 and the lead frame post 9 may be made of metal or other materials as known in the art.

[0014] As shown in Fig. 1, because at least one of a pair of bond wires 11, 12 is insulated, first bond wire 11 and second bond wire 12 can cross at bond wire crossing 13. The insulating material between the insulated bond wires 11, 12 may prevent current from shorting between one insulated bond wire to the other. If both of the bond wires 11, 12 were not coated in the insulating materials, a short may occur at the bond wire crossing 13 where the bond wires 11, 12 may be touching. The first bond wire 11 may be connected to the integrated circuit 3 and the substrate 2 by a first end connected to bond pad 24 and a second end connected to a bond pad 25. The bond wire 12 may be connected to the integrated circuit 3 and the substrate 2 by a first end connected to bond pad 23 and a second end connected to a bond pad 26. Without insulating material the short may have had to be prevented by redesigning the integrated circuit 3 or the underlying substrate 2. Either the bond pads 23, 24 may have had to be switched or lead frame posts 25, 26 may have had to be switched. The bond wires 11, 12 may allow the integrated circuit 3 and the underlying substrate 2 to be connected without having to be redesigned.

[0015] Insulating material can be coated onto bare bond wires using several possible methods. Fig. 2 shows a flowchart of one embodiment of a method to coat the insulating material onto the bare bond wire. At block 50, a machine may extrude the bare bond wire using methods known in the art. The bare bond wires may have diameters in the range of approximately 0.5 to 2 mils. However, other bare bond wire diameters may be used. At block 51, liquid insulating material may be coated onto the bare bond wire as the bare bond wire is being extruded or, in another embodiment of the invention, the bare bond wire may be extruded and then dipped or pulled through a bath of the liquid insulating

material. At decision block 52, a manufacturer may determine whether to cure or cool the insulating material based on what the insulating material is. For example, if the insulating material is a thermoset polymer, at block 54, the insulating material may be cured on the bare bond wire to form an insulated coating. The insulating material may also be cooled
5 on the bare bond wire at block 53. At block 55, the manufacturer may dry the insulating material, if needed, after the insulating material has been cooled or cured. Other methods of coating the insulating material on the bare bond wire not described herein are also within the scope of the invention.

[0016] The thickness of the insulating material connected to the bare bond wires may
10 vary depending on factors such as, but not limited to, the thickness of the bare bond wire and the type of insulating material used. The insulated bond wires in contact after installation on the integrated circuit should have a sufficient thickness of the insulating material connected to them to prevent shorts. For example, if a polymer is used as the insulating material, a thickness in the range of approximately 0.2 micrometers to 0.6
15 micrometers may be used. However, other insulating material thicknesses may also be used.

[0017] Referring to Fig. 3, an embodiment of the invention having multiple integrated circuits connected to an underlying substrate is shown. First integrated circuit 3 may be connected to second integrated circuit 4 through first insulated bond wire 27 and second insulated bond wire 28. Second integrated circuit 4 may also be connected to the underlying substrate 2 by the insulated bond wire 22. The underlying substrate 2 may also be another integrated circuit. With several integrated circuits 3, 4 forming an integrated circuit assembly, the number of potential insulated bond wire crossings may increase. As shown in Fig. 3, the insulated bond wire 22 may cross other insulated bond wires on the
20 integrated circuit assembly at bond wire crossings 19, 20, 21. Also, the insulated bond wire may cross other bond wires that do not have insulating material on them. The insulating material on one of two crossing bond wires should prevent a short between them. If the insulated bond wire 22 did not have insulating material coating it, the integrated circuits 3, 4 and the underlying substrate 2 may have had to be redesigned. The
25 bond pads on the integrated circuits and the lead frame posts on the underlying substrate 2 may have needed to be shifted to prevent the bond wire crossings 19, 20, 21. The redesign may have required extensive cooperation between the manufacturers of the integrated circuits 3, 4 and the manufacturers of the underlying substrate 2.

[0018] Also, as seen in Fig. 3, if the insulated bond wire 22 sags into an integrated circuit board edge 38, the insulating material coating the bond wire 22 may prevent the bond wire 22 from shorting into the integrated circuit board edge 38. Integrated circuits may be grounded so that the bare bond wire touching the integrated circuit board edge 38
5 may short. Bond wires may sag on the integrated circuit or if hot plastic is molded onto the integrated circuits 3, 4, the bare bond wire may be pushed into the integrated circuit board edge 38 even if it is not sagging. The insulating material on the insulated bond wires may prevent the bond wire 22 from sagging into or being pushed into the integrated circuit board edge 38 by the hot plastic. The insulating material may need to be made
10 thick enough that the integrated circuit board edge 38 will not be able to cut all the way through the insulating material and make contact with the bond wire 22.

[0019] Because insulating material may keep the bond wires from shorting to each other or the integrated circuit board edge 38, bond wire pitch angle 39 may be made smaller. Without the insulating material, the bond wire pitch angles 39 may need to be great
15 enough to prevent the bond wires from contacting other bond wires or the integrated circuit board edge 38. With the insulating material, the insulated bond wires may be able to touch each other and the integrated circuit board edge 38, and therefore, the bond wire pitch angles 39 may be made tighter. Tighter bond wire pitch angles may mean the integrated circuit assembly's final size can be smaller.

[0020] Referring to Fig. 4, a close-up of a ball bond on an embodiment of the invention is shown. Insulated bond wire 5 is connected to lead frame post 9 through ball bond 8. In one embodiment of the invention, the ball bond 8 may be formed with an ultrasonic bond between an end of insulated bond-wire 7 and the lead frame post 9. Insulating material 6 may be removed from the insulated bond wire 7 a distance 18 from the end of the bond wire 7. The insulated bond wire 7 without the insulating material on its ends may bond better to the bond pads or the lead frame posts 9, however, the insulated bond wire 7 may also be connected to the bond pads or the lead frame posts 9 with the insulating material on its ends. The distance 18 may be in the range of approximately 0 to 20 microns or approximately five percent of the bond wire's total length. However, other distances 18 of
25 the insulating material may be removed. In one embodiment of the invention, the insulating material 6 vaporizes off of the end of the bond wire 7 during the ultrasonic bonding process. In another embodiment of the invention, the insulating material 6 is stripped off of the end of the bond wire 7 before the ultrasonic bond is formed. A
30

capillary may be used to cut and strip the end insulating material 6 off. Other methods of stripping the insulating material 6 off of the end of the bond wire 7 are within the scope of the invention. In another embodiment of the invention, a solvent may be applied to the end of the insulated bond wire 5 to dissolve the insulating material 6 off of the end of the bond wire 7.

[0021] Referring to Fig. 5, an embodiment of the invention having two integrated circuits connected to each other and an underlying substrate 2 through insulated bond wire is shown. If bond wires 29, 30 are coated in an insulating material, such as a polymer, distance 16 between the adjacent insulated bond wires 29, 30 may be smaller than if the bond wires 29, 30 were not coated in the insulating material. The insulating material coating the bond wires 29, 30 may inhibit electronic interference between the bond wires 29, 30 to allow the bond wires 29, 30 to be brought closer together. Because the distance 16 can be decreased, distance 17 between lead frame posts 34, 35 may also be decreased. Because the lead frame posts on the underlying substrate 2 can be brought closer together, the underlying substrate 2 may be capable of holding more lead frame posts and correspondingly have more outlets for input and output. The increased number of the outlets may increase the functionality of the underlying substrate 2. Alternately, the underlying substrate 2 may be made smaller without losing its current level of functionality if it can place the lead frame posts closer together.

[0022] In the same way, distance 14 between insulated bond wires 31, 32 may be smaller than if the insulated bond wires 31, 32 were not coated in the insulating material. Because distance 14 can be minimized, distance 15 between bond pads 36, 37 may also be minimized. The reduced space between the bond pads on the integrated circuit 3 means more bond pads may fit on the integrated circuit 3 and thereby increase the functionality of the integrated circuit 3.

[0023] Insulated bond wires may increase reliability and flexibility for integrated circuits and integrated circuit designs. Insulated bond wires may cross other insulated bond wires, touch other insulated bond wires, or touch an integrated circuit board edge without shorting. These features of insulated bond wires may allow integrated circuits to attach to each other and other substrates with crossed bond wires where before, the integrated circuits or substrates may have had to be redesigned to prevent crossed wires. Insulated bond wires may also allow for smaller or more functional integrated circuits by

allowing insulated bond wires to be closer together without electronically interfering with each other.

[0024] Although an exemplary embodiment of the invention has been shown and described in the form of insulated bond wires, many changes, modifications, and substitutions may be made without departing from the spirit and scope of the claimed invention.

CLAIMS

We claim:

1. An apparatus comprising:
 - a bond wire;
 - 5 an insulating material coating said bond wire; and
 - a first end of said bond wire connected to a bond pad.
2. The insulated bond wire of claim 1 wherein said bond wire material is selected from a group consisting of gold, silver, aluminum, and copper.
- 10 3. The insulated bond wire of claim 1 wherein said insulating material is comprised of a polymer.
4. The insulated bond wire of claim 1 wherein the thickness of said insulating material on said bond wire is in the range of approximately 0.2 micrometers to 0.6 micrometers.
- 15 5. The insulated bond wire of claim 1 wherein said bond wire is connected to said bond pad through an ultrasonic bond.
6. The insulated bond wire of claim 1 further comprising said bond pad connected to an integrated circuit.
- 20 7. The insulated bond wire of claim 1 further comprising said bond pad connected to a substrate.
8. An integrated circuit comprising:
 - a first bond wire;
 - an insulating material coating said first bond wire;
 - 25 a first end of said first bond wire connected to a bond pad; and
 - a second bond wire crossing said first bond wire.
9. The pair of bond wires of claim 8 further comprising an insulating material coating said second bond wire.

10. The pair of bond wires of claim 8 wherein said first bond wire touches said second bond wire.
11. An integrated circuit assembly comprising:
 - 5 an integrated circuit;
 - a substrate;
 - a bond wire connected to said integrated circuit and said substrate; and
 - an insulating material coating said bond wire.
12. The integrated circuit assembly of claim 11 wherein said substrate is selected from a group consisting of printable circuit boards, aluminum lead frames, and fine pitch ball grid arrays.
- 10
13. The integrated circuit assembly of claim 11 wherein said insulating material is comprised of a polymer.
14. The integrated circuit assembly of claim 11 wherein said bond wire material is selected from a group consisting of gold, silver, aluminum, and copper.
- 15
15. An integrated circuit assembly comprising:
 - 15 a first integrated circuit;
 - a second integrated circuit;
 - a bond wire connected to said first integrated circuit and said second integrated circuit; and
- 20
- an insulating material coating said bond wire.
16. The integrated circuit assembly of claim 15 wherein said substrate is selected from a group consisting of printable circuit boards, aluminum lead frames, and fine pitch ball grid arrays.
17. The integrated circuit assembly of claim 15 wherein said insulating material is comprised of a polymer.
- 25

18. The integrated circuit assembly of claim 15 wherein said bond wire material is selected from a group consisting of gold, silver, aluminum, and copper.
19. A method of connecting a bond wire to a bond pad comprising:
 - 5 providing a bond wire;
 - coating an insulating material to said bond wire; and
 - connecting a first end of said bond wire to a bond pad.
20. The method of claim 19 further comprising removing said insulating material from said first end of said bond wire.
21. The method of claim 19 wherein said connecting an insulating material to said bond wire comprises:
 - 10 coating said bond wire in liquid insulating material; and
 - curing said liquid insulating material on said bond wire.
22. The method of claim 19 wherein said connecting an insulating material to said bond wire comprises:
 - 15 coating said bond wire in liquid insulating material; and
 - cooling said liquid insulating material on said bond wire.
23. The method of claim 20 wherein said insulating material is removed from said first end of said bond wire by vaporization.
24. The method of claim 20 wherein said insulating material is removed from said first end of said bond wire by stripping.
25. The method of claim 20 wherein said insulating material is removed from a first end of said bond wire by dissolving said insulating material off said first end of said bond wire with a solvent.
26. The method of claim 21 further comprising drying said coated insulating material.
27. The method of claim 22 further comprising drying said coated insulating material.

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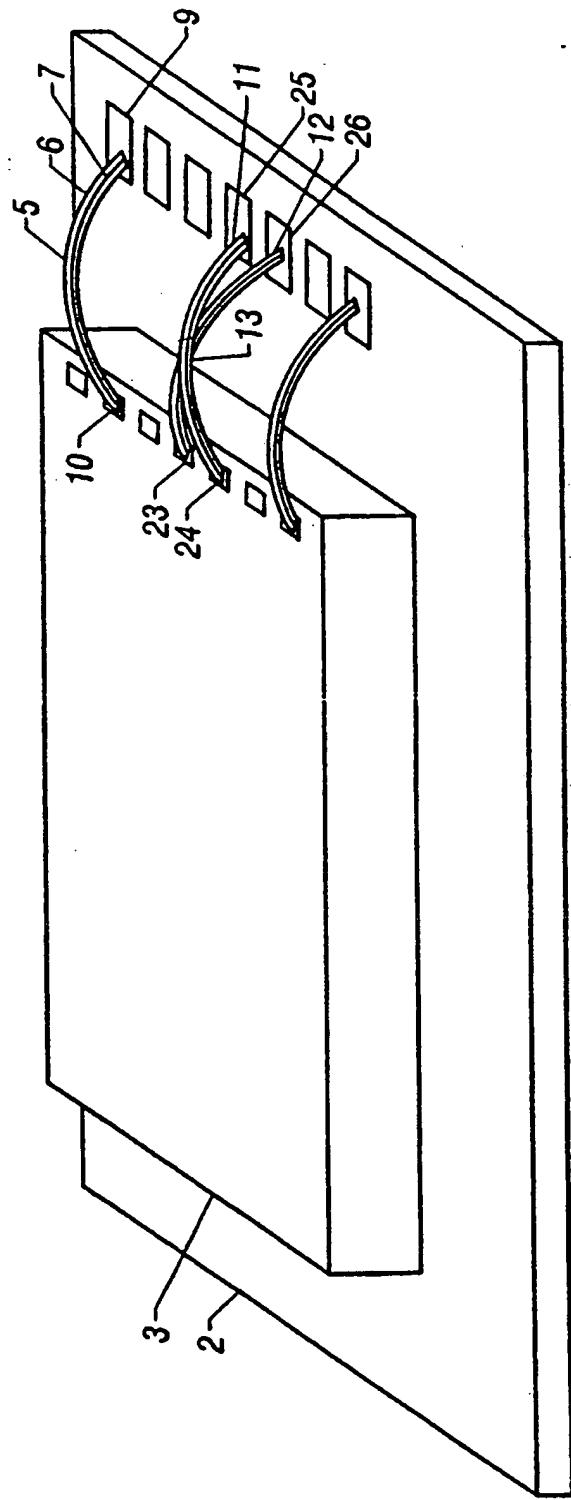


FIG. 1

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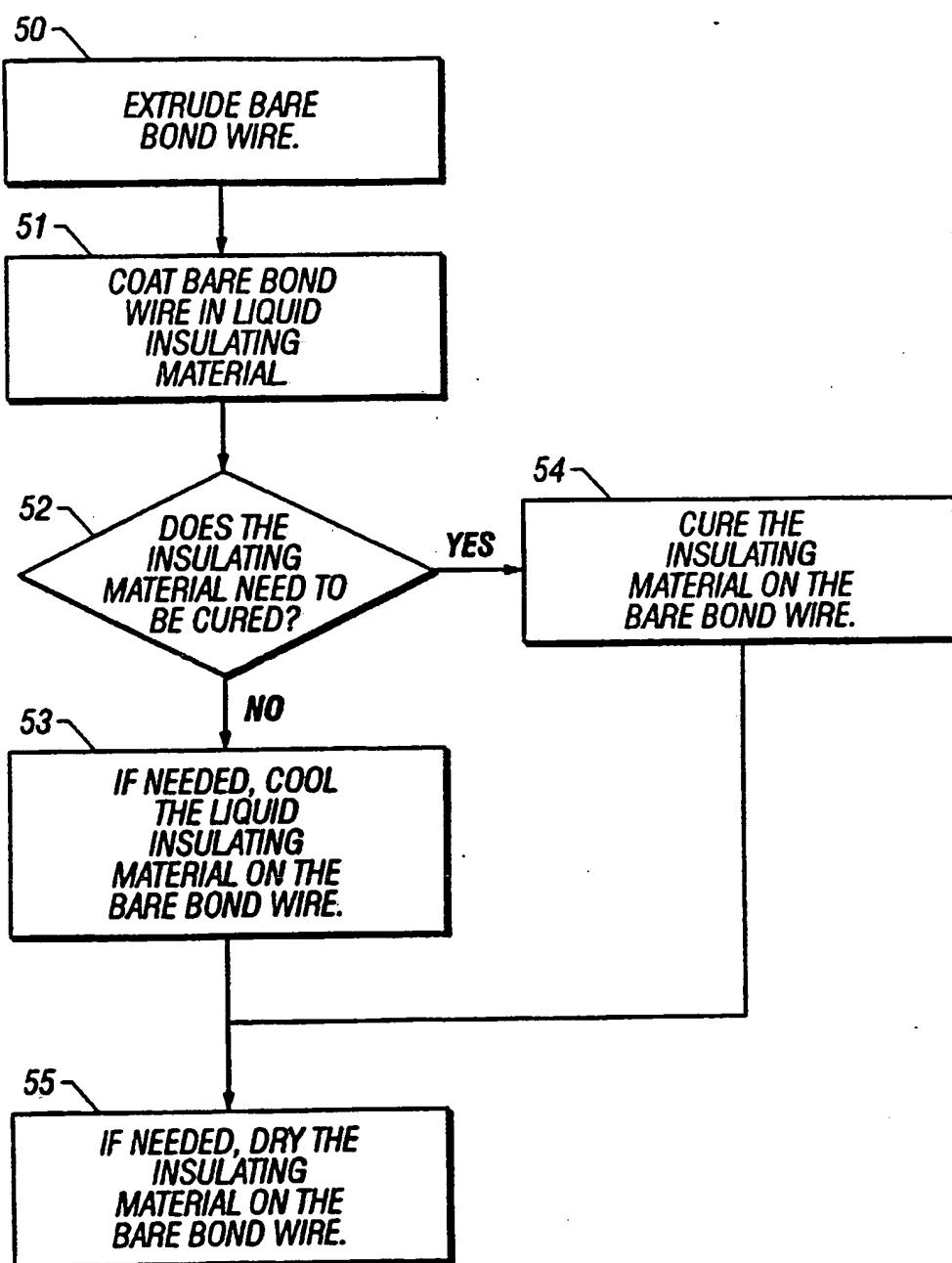


FIG. 2

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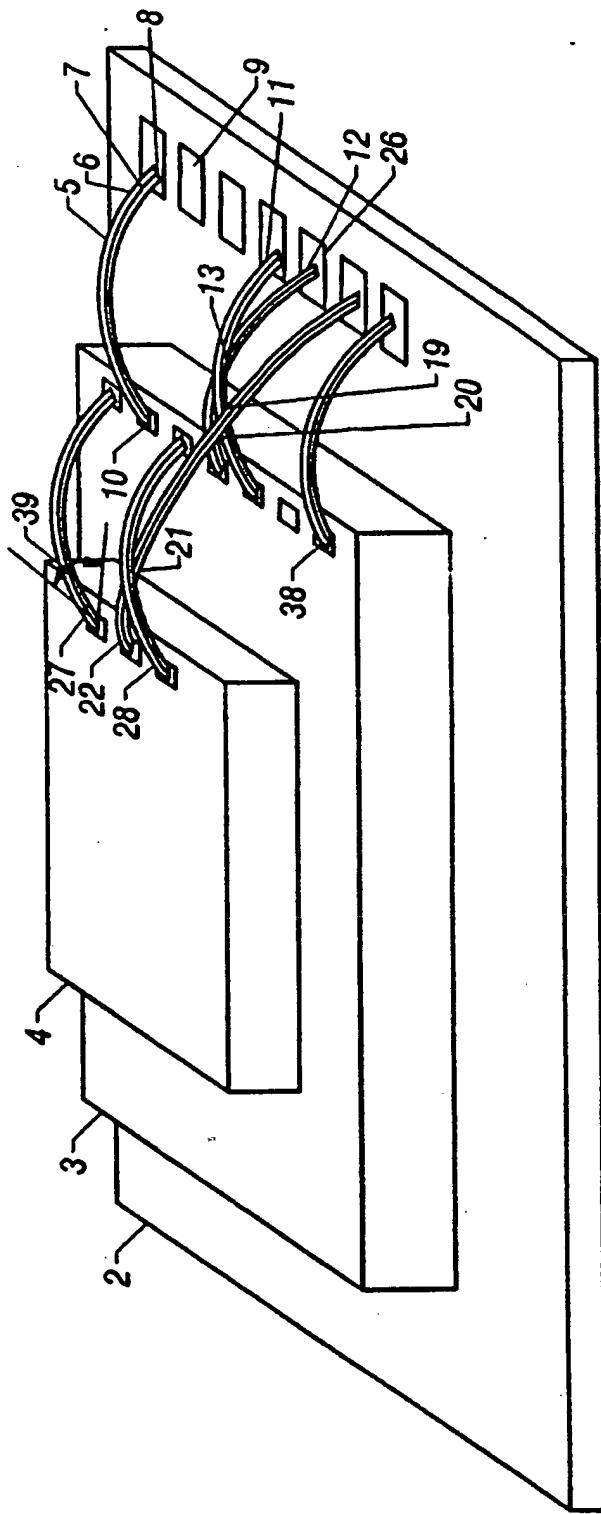


FIG. 3

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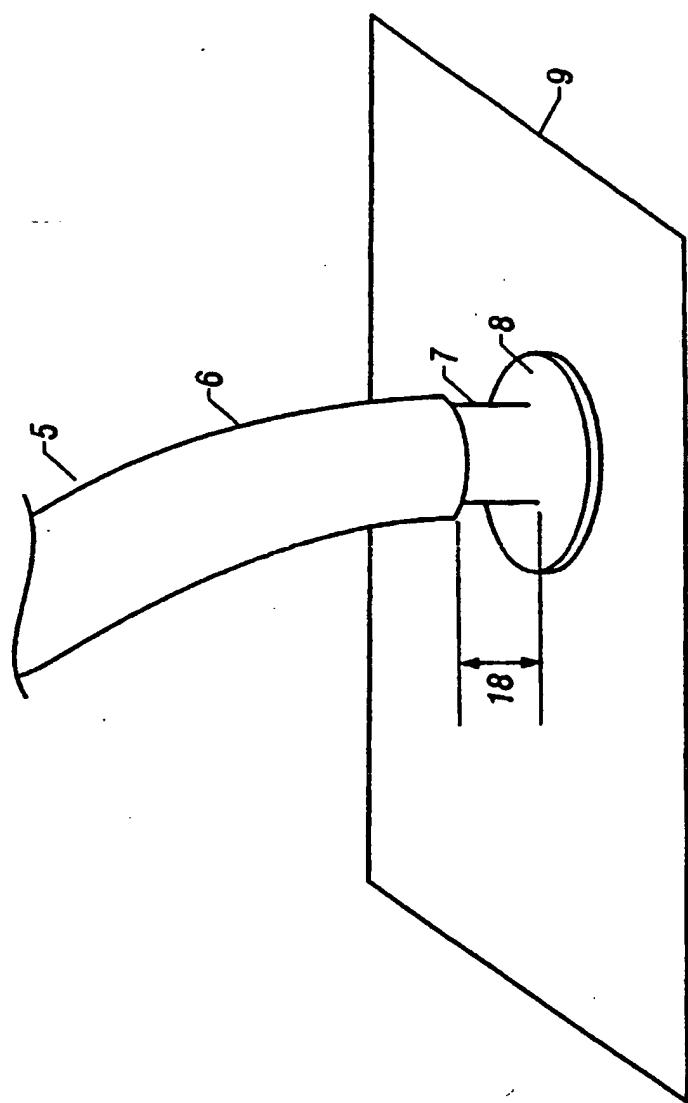


FIG. 4

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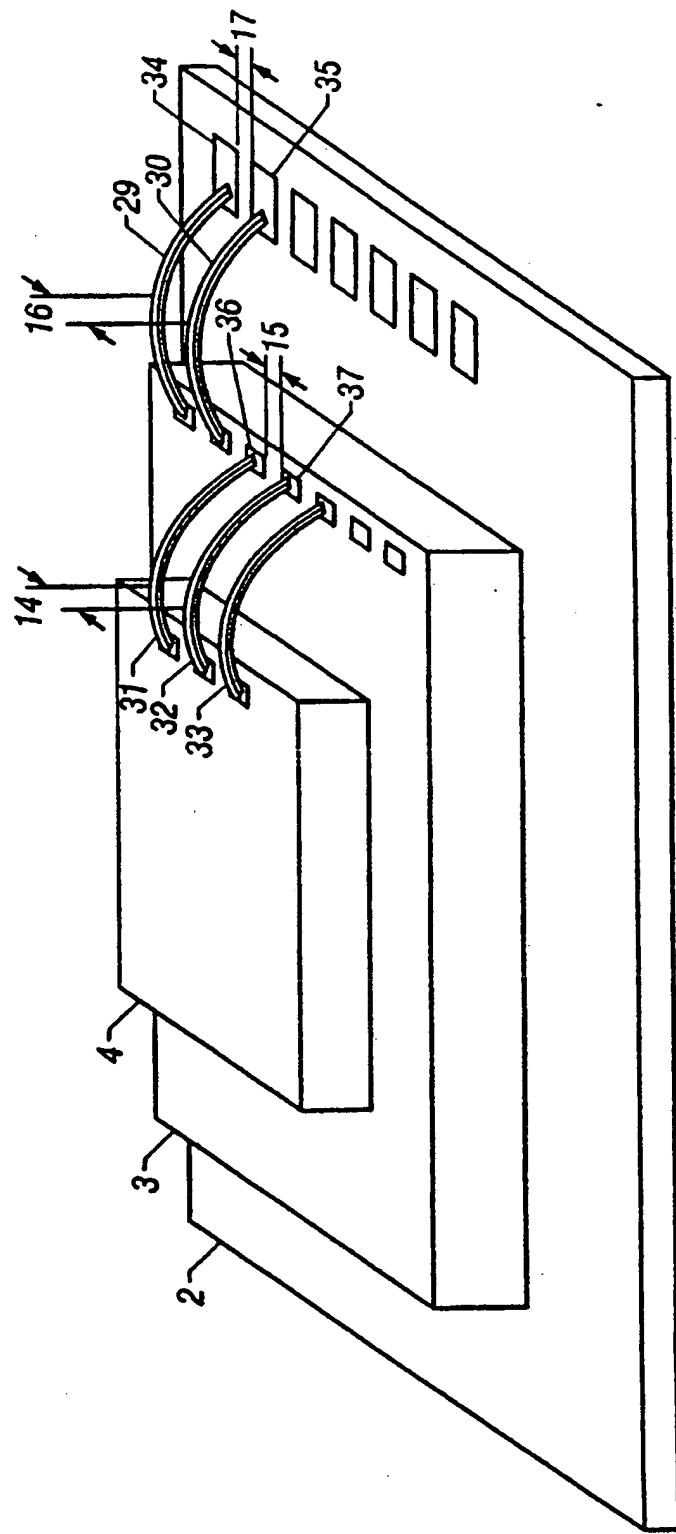


FIG. 5

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AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU,
CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH,
GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC,
LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW,
MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG,
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European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR,
GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent
(BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR,
NE, SN, TD, TG).

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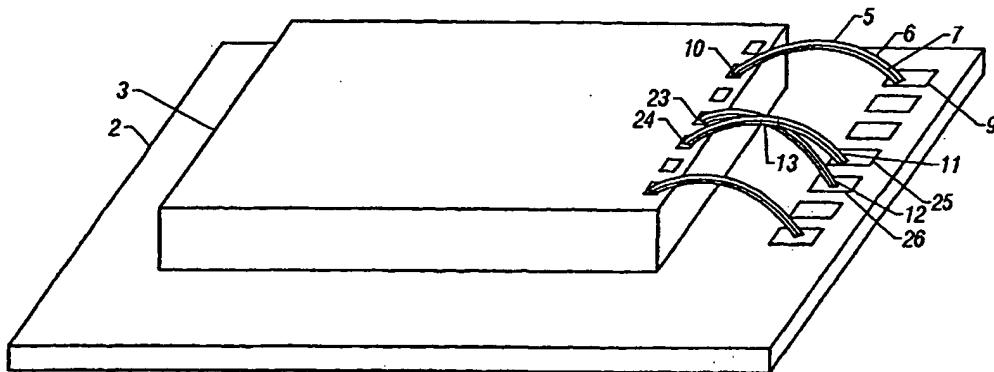
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B. FIELDS SEARCHEDMinimum documentation searched (classification system followed by classification symbols)
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No. --
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A	the whole document	8
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
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Information on patent family members

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